REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated June 1, 2006. By the present Amendment, each of the independent claims 1, 5 and 9 has been amended to clarify the invention as will be discussed in detail below.

Briefly, the present invention is directed to an improved semiconductor integrated circuit which generates an internal clock signal to be used for fetching input data synchronously with the internal clock signal. As discussed in the Background of the Invention, with regard to Fig. 16, prior systems for synchronizing the input of data with an internal clock signal have been developed which operate satisfactorily when a duty ratio of an input clock signal CK is 50% (in other words, when, as shown in Fig. 16, the time period th equals tl). On the other hand, as discussed beginning at the bottom of page 2 of the Specification with regard to Fig. 17, if the duty ratio of the clock signal CK is different than 50% (for example, 70% in the example shown in Fig. 17) an adequate timing margin cannot be assured. Accordingly, as set forth on page 3, line 5 et seq., of the Specification:

> "An object of the present invention is to prevent the timing margin, at the time of latching the data signal synchronously with the clock signal, from being decreased in the case where the duty ratio of the clock signal CK is different from 50%."

Fig. 1 represents one embodiment of the present invention to achieve this object. In Fig. 1, the input terminal DI receives a data input while a clock input

terminal receives clock signals CKT and CKB. Internal clock generating circuits DLLT and DLLB are provided to generate internal clocks CKIT and CKIB to latch circuits DIRG. In particular, the internal clock generating circuits are constructed to avoid the problem of the decrease of the timing margin discussed above. Specifically, as set forth in the last paragraph of page 3 of the Substitute Specification:

> "According to this aspect of the invention, the data signal is fetched synchronously with the internal clock signal which is switched at an intermediate timing between the i-th switch timing and the (i+1)th switch timing of the clock signal input to the clock input terminal. Thus, even in the case where the duty ratio of the clock signal is different from 50%, the timing margin for fetching data can be prevented from being reduced."

Reconsideration and allowance of the amended independent claims 1, 5 and 9 over the cited prior art to Coteus (USP 6,807,125), Kawasaki (USP 6,066,969) and Fujieda (USP 6,181,174) is respectfully requested. By the present Amendment each of the independent claims has been amended to include the feature of the invention that the internal clock generating circuit is constructed to include means for preventing the timing margin, at the time of latching the data signal synchronously with the internal clock signal, from being decreased in a case where duty ratio of the clock signal input from the clock input terminal is different than 50%. It is respectfully submitted that none of the cited references to Coteus, Kawasaki and Fujieda teach or at all suggest any such means for preventing a decrease in the timing margin where the duty ratio of the clock signal is different than 50%. Quite to

the contrary, the arrangements taught by these cited references have nothing whatsoever to do with preventing such a reduction of timing margin when a duty ratio of the clock signal is different than 50%.

For example, the primary reference to Coteus is directed to a method of generating a delayed clock signal (as discussed in the Abstract and shown in Fig. 1). In other words, Coteus is only interested in a system for determining an amount of delay which is appropriate (e.g., see column 2, line 42 *et seq.)* and provides no suggestion for means for preventing a timing margin at a time of latching a data signal from being decreased in a case where the duty ratio of the clock signal is different than 50%.

In the Office Action, reference is made to Fig. 3 of Coteus for the original claim limitations (still found in the amended claim) regarding the generating of the internal clock signal such that the internal clock signal is switched at an intermediate time in between the i-th switch timing and the (i+1)th switch timing. In Fig. 3, the switch (rise) timing of the signal dqs_clk is arranged in the middle of a rise timing and a following fall timing of DQS while a switch (rise) timing of dqsn_clk is arranged in the middle of a fall timing and a following rise timing of DQS. However, as noted above, this has noting to do with the feature of the present claimed invention for providing the claimed switching in an intermediate timing in order to prevent a timing margin from being decreased in a case where the duty ratio of the clock signal is different than 50%.

Similarly, Kawasaki is directed to a clock arrangement for a data output, but completely fails to teach or suggest any means for preventing a timing margin from being decreased in a case where a duty ratio of a clock signal input is different than 50%. Kawasaki is merely of general interest with regard to a teaching of a DLL circuit which adjusts a delay of a variable-delay circuit. This DLL circuit includes a delay-control circuit (18) which adjusts the delay of the variable-delay circuit, and a clock selection circuit (30) which controls the clock-control circuit to select one of an input clock signal (i-clk) and the delayed clock signal (d-dll-clk). The variable-delay circuit is controlled so that the delay is not increased when the input clock signal is selected by the clock selection circuit 30. Although this may be of general interest, there is no suggestion whatsoever of means for preventing a timing margin from being decreased in a case where a duty ratio of the clock signal is different than 50% by including means for switching the internal clock signal at the claimed intermediate timing.

Finally, the Fujieda reference is simply of general interest with regard to teaching a clock for a data output, and, like the above discussed references to Coteus and Kawasaki, completely lacks any suggestion of the claimed means for preventing a timing margin from being decreased in a case where the duty ratio of the clock signal is different than 50%.

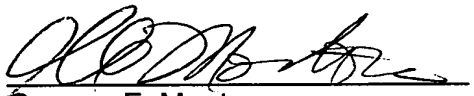
For the reasons set forth above, it is respectfully submitted that the amended claims clearly define over the cited references to Coteus, Kawasaki and Fujieda,

and, for these reasons, reconsideration and allowance of the amended independent claims 1, 5 and 9 and their respective dependent claims is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 1374.43352X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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